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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
VIDA, MELANIE M	
ART UNIT	**PAPER NUMBER**
2697	6

DATE MAILED: 05/23/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/389,048	ADACHI ET AL.	
	Examiner	Art Unit	
	Melanie M Vida	2697	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 September 1999* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 September 1999* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

I.

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on 9/2/99 has been considered by the examiner and is attached to this office action.

II.

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

III.

Drawings

1. New corrected drawings are required in this application because the drawings must be translated from Japanese to English. Applicant is advised to employ the services of a competent patent draftsperson outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings. The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

2. **Figure 2, 23, 48** should be designated by a legend such as --Prior Art-- because only that which is old is illustrated as mentioned in the specification (Pg. 2, lines 17-18), (Pg. 21, lines 3-4) & (Pg. 23, lines 21-22). See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

IV.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

2. The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

3. **Claims 3, 10, 14, 15, 21, 29,** and **30** recite the limitation that lack proper sufficient antecedent basis. The Examiner list the following examples:

a. "data read means" in claim 3, (Pg. 100, line 1);

b. "a second register" in claim 10, (Pg. 103, lines 9-10);

c. "the threshold data read step" in claim 14, (Pg. 104, line 23); claim 15, (Pg. 105, line 20); claim 29, (Pg. 114, line 10); claim 30, (Pg. 115, line 6);

d. "the step" in claim 14, (Pg. 105, line 1); claim 15, (Pg. 105, line 24); claim 30, (Pg. 115, line 10, line 19);

e. "the threshold data selection step" in claim 14, (Pg. 105, line 4); claim 15, (Pg. 106, line 2); claim 29, (Pg. 114, line 14); claim 30, (Pg. 115, line 13);

f. "the comparison step" in claim 14, (Pg. 105, line 9); claim 15, (Pg. 106, line 7); claim 29, (Pg. 114, line 19); and claim 30, (Pg. 115, line 21).

g. "the later" in claim 21, (Pg. 110, line 20, and line 22).

4. **Claim 1-37** is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The shift register (11p), (12p), and (2p) as disclosed in the specification (Pg. 45, lines 7-24) is ambiguous with the terminology in the claim language as follows: The following

terms in the claims 1-37 is used by the claim to mean "shift register", while the accepted meaning is "shift register (11p)", shift register (12p)" and "shift register (2p)", respectively.

a. "first register means" (claim 1, Pg. 98, line 11; claim 2, Pg. 99, line 10; claim 5, Pg. 101, line 6; claim 6, Pg. 101, line 14; claim 7, Pg. 101, line 23-24; claim 10, Pg. 103, line 22; claim 14, Pg. 105, line 3, 7; claim 15, Pg. 106, line 5; claim 19, Pg. 109, line 5; claim 30, Pg. 115, line 12, line 17,);

b. "second register means" (claim 3, Pg. 100, line 1 and line 11; claim 4, Pg. 100, line 22; claim 10, Pg. 103, line 9; claim 19, Pg. 109, line 14; claim 30, Pg. 115, line 20, line 23-24);

c. "second register in the preceding stage", (claim 10, Pg. 103, line 9-10);

d. "second register in the following stage", (claim 10, Pg. 103, line 10-11, line 14-15; line 19, line 21-22);

Thoroughly review all the claims 1-37, and correct all improper claims for the format described above.

5. The term "the later of the M threshold data" in claim 21 is a relative term which renders the claim indefinite. The term "the later of the M threshold data" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. The M threshold data is less than P, and the addition of the later plus the threshold data pieces consecutive starting at the top are unclear in the claim, (Pg. 110, lines 20-25).

V.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

2. A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. **Claim 1, 13, 14, 18** is rejected under 35 U.S.C. 102(e) as being anticipated by Lapstun U.S. Patent 6,512,596 B1, (hereinafter, Lapstun).

Regarding **claim 1**, as shown in figure 24, Lapstun discloses a halftoner/compositor (HCU), (141), which reads on a halftone generation system, (col. 35, lines 65-67), wherein it, (141) a contone CMYK image layer is halftoned to a bi-level CMYK layer, which reads on generating halftone data of a pixel, (col. 35 line 65- col. 36, line 2). As shown in figure 26, a series of contone color pixel values is input to four separate triple threshold units (204), (col. 37, lines 41-44), wherein a clock enable generator (206) generates enable signals for clocking the contone CMYK pixel input, and the CMYK dot output, which reads on generating halftone data

of a pixel based on a comparison between multilevel image data of the pixel and threshold matrix data, (Table 21; col. 38, lines 11-15). The halftoner/compositor (HCU), which reads on the halftone generation system comprises:

a. A dither cell ROM, read on threshold matrix data storage means, is accessed to retrieve three thresholds in a 24-bit value format from a 64x64x3x8-bit dither volume, reads on storing threshold matrix data, (col. 37, lines 21-24).

b. If dither cell registration is chosen, then triple threshold value can be retrieved once and used to dither each color component. Otherwise, if dither cell registration is not desired, then the dither cell can be split into four sub-cells and stored in four separately addressable ROMS from which four different triple, threshold values can be retrieved in parallel in one cycle, which reads on threshold data read means for reading all threshold data applied to halftone data generation processing, (col. 37, lines 25-32). As shown in figure 24, the input to the HCU is an expanded 267 ppi CMYK contone layer (200), and an expanded 1600 dpi black layer (201). The output from the HCU is a set of 1600 dpi bi-level CMYK image lines (202), which reads on halftone generation processing. This is inherently done for each scanning line as evidenced that the input contone CMYK FIFO is a full 8 KB line buffer, and the output stage of the HCU uses 8 parallel pixel FIFO's, one for each for even cyan, odd cyan, even magenta, odd magenta, even yellow, odd yellow, even black, and odd black, (col. 36, lines 60-65). The contone data is dithered using a triple threshold dither volume, where the three thresholds form a convenient 24-bit value, which can be retrieved from the dither cell ROM in one cycle, which reads on from said threshold matrix data storage means, (col. 36, lines 1-6; col. 37, lines 21-24).

c. If dither cell registration for each color plane is not desired, then the dither cell can be split into four-subcells and stored in four separately addressable ROMs from which four different triple-threshold values can be retrieved in parallel in one cycle. As shown in figure 26 four gates indicated generally by **207**, which reads on first register means, has input from the four dither subcells, A, B, C, D, which reads on retaining all the read threshold data. The threshold data is output from the four gates, as shown in figure 26, to a series of four, triple-threshold value units, (col. 37, lines 35-40). The multi-threshold dither (203) and the triple-threshold unit (204) converts a triple-threshold value and an intensity value into an interval and thence a one or zero bit as shown in table 21, which reads on applied to halftone data generation processing, (col. 37, lines 35-40).

This is inherently done for each scanning line as evidenced that the input contone CMYK FIFO is a full 8 KB line buffer, and the output stage of the HCU uses 8 parallel pixel FIFO's, one for each for even cyan, odd cyan, even magenta, odd magenta, even yellow, odd yellow, even black, and odd black, (col. 36, lines 60-65).

d. As shown in figure 26, a dither cell address generator and four gates indicated generally at **207,** control the retrieval of the four different triple threshold values, which reads on a threshold data selection means (col. 37, lines 45-50). The dither volume is a triple-threshold 64x64x3x8-bit volume, which is split into four subcells A, B, C, D, indicated generally at **205** in figure 26, which reads on selecting a plurality of threshold data pieces from among the threshold data pieces, (col. 37, lines 5-8; col. 37, lines 43-46). The multi-threshold dither (203) and the triple-threshold unit (204) converts a triple-threshold value and an intensity value into an interval

and thence a one or zero bit as shown in table 21, which reads on applied to halftone data generation processing, (col. 37, lines 35-40).

This is inherently done for each scanning line as evidenced that the input contone CMYK FIFO is a full 8 KB line buffer, and the output stage of the HCU uses 8 parallel pixel FIFO's, one for each for even cyan, odd cyan, even magenta, odd magenta, even yellow, odd yellow, even black, and odd black, (col. 36, lines 60-65).

As shown in figure 26, four gates indicated generally by **207**, which reads on first register means, has input from the four dither subcells, A, B, C, D, which reads on retaining all the read threshold data, The output of the four gates (207), is the threshold data, (A, B, C, D), (B, C, D, A), (C, D, A, B), and (D, A, B, C), as shown in figure 26, to a series of four triple threshold units (204), which reads on outputting the selected threshold data pieces, (col. 37, lines 35-40).

e. As shown in figure 26, the series of four triple threshold units (204), read on a plurality of comparison means, uses triple-thresholding rules as shown in Table 21, figure 27, reads on a comparison processing, (col. 37, lines 35-40). As shown in table 21 and figure 26-27, the triple-threshold unit (204) converts a triple-threshold value, read on between threshold data pieces, input by a dither cell address generator, (206), read as selected by said threshold data selection means, and an intensity value, read on multilevel image data of a plurality of pixels. The input from the four different triple threshold values can be retrieved in parallel in one cycle for the different colors into an interval, read on a plurality of pixels in parallel and executing parallel generation, and thence a one or zero bit, which reads on halftone data of the pixels (col. 37, lines 35-40; col. 37, lines 45-50; Table 21, Figure 26-27).

Regarding **claim 13**, as shown in figure 26, four triple threshold units (207) accepts a plurality of threshold data, (A, B, C, D), read on the threshold data read means, reads a plurality of threshold data pieces at the same time. The threshold data is from the four ROM dither subcells (203), read on the threshold matrix data storage means.

Regarding **claim 14,** please refer to the like teachings of claim 1.

Regarding **claim 18,** please refer to the like teachings of claim 1.

VI.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. **Claim 2, 15** is rejected under 35 U.S.C. 103(a) as being unpatentable over Lapstun U.S. Patent 6,512,596 B1.

Regarding **claim 2**, please refer to the like teachings of claim 1, and further where Lapstun does not expressly disclose that the halftone generation system for generating halftone data of a pixel based on comparison between multilevel image data of the pixel and threshold matrix data in painting object units.

Lapstun further does not expressly disclose that the threshold data read means reading all threshold data applied to halftone data generation processing for one scanning line from said threshold matrix data storage means in response to the start position of a painting object.

However, Lapstun teaches, as shown in figure 2, "render contone image and graphics", and "render black text and graphics, is read on painting object units in the halftone generation system. Further, since this step is shown prior to the "halftone contone data", it reads on a threshold data read means in response to the start position of a painting object.

It would have been obvious to anyone of ordinary skill in the art at the time of the invention to modify the halftone generation system with Lapstun's disclosure of a graphics system to "render contone image & graphics" and "render black text and graphics", and further to start a threshold read means in response to the start position of a painting object.

One of ordinary skill in the art would have been motivated to do this because the method is optimal for painting objects instead of text.

Regarding **claim 15,** please refer to the like teachings of claim 2.

3. **Claim 3, 4, 12, 16, 17, 19, 20, 29, 30** are rejected under U.S.C. 103(a) as being unpatentable over Lapstun U.S. Patent Number 6,512,596 B1 as applied to claim 1 above, and further in view of Mannichi et al. U.S. Patent Number 5,161,036 (hereinafter, Mannichi) and further in view of well-known prior art (MPEP 2144.03).

Referring to **claim 3,** Lapstun teaches all the features of the halftone generation system in claim 1 above, but fails to expressly disclose the following:

a. Said data read means comprises; second register means for retaining all threshold data applied to halftone data generation processing for the scanning line to be processed next to the current scanning line where halftone data generation processing is being executed;

b. Said threshold data read means reads all threshold data applied to halftone data generation processing for the scanning line to be processed next to the current scanning line from said threshold matrix data storage means, and outputs the read threshold data to said second register means;

c. The threshold data retained in said second register means is output to said first register means.

However, as shown in figure 1, Mannichi teaches of a picture digitizing system, read on a halftone generation system, wherein an input picture signal obtained through the line scanning operation, read on a data read means, of a halftone picture is converted to digital data of n bits through an A/D converter, (11) (col. 5, lines 20-30). The digital data is compared through a comparator (12) with binary threshold data of n bits received from a read-only memory (13) ROM. The comparator (12) outputs binary digital data corresponding to the input picture signal. In order to address threshold data, the ROM (13) receives address information based on 12 parallel, binary picture signals, and m-bits randomly number generated from a random number generator (14), (col. 5, lines 30-40). The ROM (13) outputs the aforementioned binary threshold data to the comparator (12), as shown in figure 1. Mannichi further illustrates a series of shift registers, (15), (16), (17), (18), (19), read on a second register means, which outputs in conjunction with data from a random digital generator (14), 12 bits of binary digital data to ROM (13), (col. 5, lines 36; col. 6, lines 12-14). The shift registers (16), (17), (18), and (19) acts to delay the one-bit digital data by one line scanning time period, read on halftone data generation processing for the scanning line where halftone data generation processing is being executed, (col. 5, lines 45-55). Mannichi teaches the threshold read means, in that the ROM (13) outputs

to the comparator (12), binary threshold data that was previously addressed by the parallel, 12-bit data from the shift registers (15)-(19), and the m-bit data from the random number generator (14), (col. 5, lines 36-42). The 12-bit data from the shift registers (15)-(19) is output in parallel based on binary data corresponding to the picture input signal, that had been delayed by one line scanning time period, read on all threshold data applied to halftone data generation processing for the scanning line to be processed, (col. 5, lines 45-59). The comparator (12), has input from the digital picture input from the A/D converter (11), that is the current scanning line, and n-bit binary threshold data, that is from the threshold matrix data storage means, and outputs binary digital data corresponding to the input picture signal, which is supplied to a shift register (15), said second register means.

At the time the invention was made it would have been obvious to a person of ordinary skill in the art to modify Lapstuns' halftone generation system to use shift register means for shifting data such as the teachings of Mannichi.

One of ordinary skill in the art would have been motivated to do this in order to create a high-speed halftone generation system.

Lapstun in view of Mannichi does not expressly disclose that the shift registers (15)-(19) store threshold data, or defines it as a second register means. Further, Lapstun in view of Mannichi also does not expressly disclose that the ROM (14) is a first register means. Finally, the prior art does not disclose that the threshold data is output from the second register is to the said first register means.

The Examiner takes Official Notice that at the time the invention was made it would have been obvious to a person of ordinary skill in the art to modify Lapstun's halftone generation

system with a first and second shift register means for manipulating threshold data prior to halftone generation based on Mannichi's teachings of a high-speed picture digitizing system using shift registers to slightly modify binary threshold data.

One of ordinary skill in the art would have been motivated to do this in order to create a high-speed halftone generation system (col. 12, lines 55-58), and further to avoid deterioration of the picture quality, (col. 2, lines 22-35), given the express suggestions of Mannichi.

Regarding **claim 4, 17,** please refer to the like teachings of claim 1 and 3.

Regarding **claim 16,** please refer to the like teachings of claim 3.

Regarding **claim 19, 30,** please refer to the like teachings of claim 1 and 3.

Regarding **claim 12,** Lapstun teaches all the features of the halftone data generation system in claim 2, but does not expressly disclose that the threshold data read means controls the number of threshold data pieces to be read from the storage means in response to the number of pixels of painting object on a scanning line to which processing is applied.

However, Mannichi teaches that 12-bit data is output from the shift register (15)-(19), and m-bits from a random number generator (14), in order to address n-bit binary threshold data from the ROM (13), read on a threshold data read means controls the number of threshold data pieces to be read from the storage means. The input to the shift registers is 1-bit binary digital signal corresponding to the original input picture signal, read on in response to the number of pixels of painting object on a scanning line to which processing is applied, (figure 1), (5, lines 35-41).

At the time the invention was made it would have been obvious to a person of ordinary skill in the art to modify Lapstun's teachings of a halftone generation system with a step for creating threshold data in response to the pixels input.

One of ordinary skill in the art would have been motivated to do this in order to create a high-speed halftone generation system.

Lapstun in view of Mannichi does not expressly disclose that the input pixel is painting objects.

The Examiner takes Official Notice that it would have been obvious to modify Lapstun in view of Mannichi's halftone generation system/method for digitizing picture signals for a halftone generation system for paint objects.

One of ordinary skill in the art would have been motivated to do in order to create a high-speed application for paint objects using a similar method for picture signals.

Regarding **claim 20,** Mannichi further teaches that the ROM (13), as shown in figure 1, read on the threshold data read means, outputs a n-bit binary threshold signal, read on reads all the threshold data, and compares it with an n-bit A/D input picture signal, read on applied to scanning line for generating a halftone from said threshold matrix data storage means for storing matrix data by accessing memory once, (col. 4, lines 30-41).

Regarding **claim 29,** please refer to the like teachings of claim 1 and 3.

VII.

Allowable Subject Matter

1. **Claim 4-11, 21-28, 26, 31-32, 35-37** would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include

all of the limitations of the base claim and any intervening claims. **Claim 4** is allowable for output processing of the read threshold data to said second register means is performed in parallel. **Claim 9** is allowable for specifying a threshold shift amount for said second register means. **Claim 22** is allowable for the select or sorting of threshold data responsive to pixel position. **Claim 24** is allowable for a threshold data selection comprising a crossbar switch circuit and a switch control circuit. **Claim 25** is allowable for shift control circuit controls the shift amount of the M threshold data pieces input to said barrel shifter circuit in response to the pixel position of generated halftone. **Claim 31** is allowable because of the "selects or sorts" all threshold data applied to the scanning line read at the threshold data read step in an arbitrary order responsive to the pixel position of generated halftone and outputs the threshold data. **Claim 35** is allowable for simultaneously reads out all the binary matrix data pieces of a scan line under processing from said data storage means in accordance with sub-scanning direction pixel position information of a painting object under processing. **Claim 36** is allowable for processing from said data storage means in accordance with main-scanning and sub-scanning direction pixel position information of a painting object under processing. **Claim 21** is allowable for threshold data selection means. **Claim 34** is allowable because of the data select means for selecting binary matrix data read out of said data reading means in accordance with main-scanning direction pixel position information of a painting object under processing. **Claim 37** is allowable for the shift of main-scanning direction pixel position of the painting object to a main-scanning direction pixel position of the binary matrix data.

VIII.

Conclusion

1. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Ueda et al. US 5,953,459 a dither matrix producing method (see col. 6).

Duffy, US 5,179,640 a shifting of pattern from a pattern header, (see figure 12, and col. 14-16).

Allebach et al. US 5,812,744 a joint design of dither matrices for a set of colorants.

Satou et al. US 5,159,471 a gate array for binary signal depending on density level of adjacent pixels (see the figures).

Curry et al. US 6,519,055 a halftoner, a thresholder (see figure 9).

Altes, US 4,802,232 a method for reducing the quantity of data in image coding.

Murakami et al. US 5,128,748 a temporary storage means for binarizing means, (see figures 6, 16, 17, 19).

Sato, U.S. Patent Number 5,073,966 for figure 5, input pixel position generates specific output dot pattern.

Miller et al. U.S. Patent Number 5,150,429 a threshold value is read out from a threshold matrix which has been modulated with a pattern which is complementary to the known artifact pattern of the error diffusion process.

2. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Melanie M Vida whose telephone number is (703) 306-4220. The examiner can normally be reached on 8:30 am 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey Hofsass can be reached on (703) 305-4717. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-6743 for regular communications and (703) 308-6743 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Melanie M Vida
Examiner
Art Unit 2697

MMV
May 19, 2003

Kimberly A. Williams
Primary Examiner
Technology Center 2600